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Generated by: Genus(TM) Synthesis Solution 17.22-s017\_1

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Module: voting\_machine

Technology libraries: tsmc18 1.0

tsmc18 1.0

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

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Instance Module Cell Count Cell Area Net Area Total Area Wireload

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voting\_machine 714 25147.584 0.000 25147.584 <none> (D)

(D) = wireload is default in technology library